

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1-7. (canceled)

8. (new) A digital data filtering circuit to correct blocking artifacts in a frequency domain within a block-based video processing device, the digital data filtering circuit comprising:

means for performing a discrete linear transform to transform a set of input luminance values, from two adjacent video segments, into a corresponding set of transformed values in the frequency domain, wherein the transformed values in the frequency domain comprise a plurality of even transformed data values and a plurality of odd transformed data values;

means for performing an inverse discrete linear transform to transform the transformed values from the frequency domain to a corresponding set of filtered values for use on a display device coupled to the video processing device; and

a control circuit coupled to the means for performing the discrete linear transform and the inverse discrete linear transform, wherein the control circuit is configured to selectively activate at least one of a plurality of filtering modules, wherein the plurality of filtering modules comprises at least one odd filtering module to filter at least one of the odd transformed data values and at least one even filtering module to filter at least one of the even transformed data values.

9. (new) The digital data filtering circuit of claim 8, wherein the control circuit is further configured to selectively activate the at least one of the plurality of filtering modules based on a predicted maximum frequency (kwpred) and a quantization step (Q).

10. (new) The digital data filtering circuit of claim 8, wherein the means for performing the discrete linear transform and the inverse discrete linear transform comprise:

a first odd filtering module (FILO1) of the plurality of filtering modules, wherein the first odd filtering module is configured to filter three of the odd transformed data values, wherein the three odd transformed data values filtered by the first odd filtering module comprises:

a first odd transformed data value having a highest frequency out of the odd transformed data values;

a second odd transformed data value having a second highest frequency out of the odd transformed data values; and

a third odd transformed data value having a third highest frequency out of the odd transformed data values; and

a second odd filtering module (FILO2) of the plurality of filtering modules, the second odd filtering module coupled to the first filtering odd module, wherein the second odd filtering module is configured to filter the first and second odd transformed data values having the highest and second highest frequencies, respectively.

11. (new) The digital data filtering circuit of claim 10, wherein the means for performing the discrete linear transform and the inverse discrete linear transform further comprise:

discrete transform means coupled to the control circuit, the discrete transform means to transform a first half of the set of input luminance values into a first half of the transformed values in the frequency domain, and to transform a second half of the set of input luminance values into a second half of the transformed values in the frequency domain; and

an even filtering module (FILE) coupled to the control circuit, wherein the even filtering module is configured to filter at least one of the even transformed data values, wherein the at least one even transformed data value filtered by the even filtering module comprises a first even transformed data value having a highest frequency out of the even transformed data values.

12. (new) The digital data filtering circuit of claim 11, wherein the even filtering module is further configured to filter the first even transformed data value and a second even transformed data value, wherein the second even transformed data value comprises a second even transformed data value having a second highest frequency out of the even transformed data values.

13. (new) The digital data filtering circuit of claim 11, wherein the discrete transform means is further configured to transform the first and second halves of the set of input luminance values into the first and second halves of the transformed values in the frequency domain, respectively, in succession at a double frequency.

14. (new) The digital data filtering circuit of claim 11, wherein the first half of the set of input luminance values comprises data of even parity from one of the two adjacent video segments, and the second half of the set of input luminance values comprises data of even parity from the other of the two adjacent video segments.

15. (new) The digital data filtering circuit of claim 11, wherein the first half of the set of input luminance values comprises data of odd parity from one of the two adjacent video segments, and the second half of the set of input luminance values comprises data of odd parity from the other of the two adjacent video segments.

16. (new) The digital data filtering circuit of claim 11, wherein the first half of the set of input luminance values comprises highest rank data one of the two adjacent video segments, and the second half of the set of input luminance values comprises lowest rank data from the other of the two adjacent video segments.

17. (new) A video decoder comprising the digital data filtering circuit of claim 8, wherein the video decoder is configured to supply filter digital images and supply decoded digital images to the display device.

18. (new) A portable apparatus comprising the digital data filtering circuit of claim 8 and the display device, wherein the portable apparatus is configured to display filtered digital images on the display device.

19. (new) A television receiver comprising the digital data filtering circuit of claim 8, wherein the television receiver is configured to filter digital images received by the television receiver and to display filtered digital images on a screen coupled to the television receiver.